

## 256K (32K x 8) UV EPROM and OTP ROM

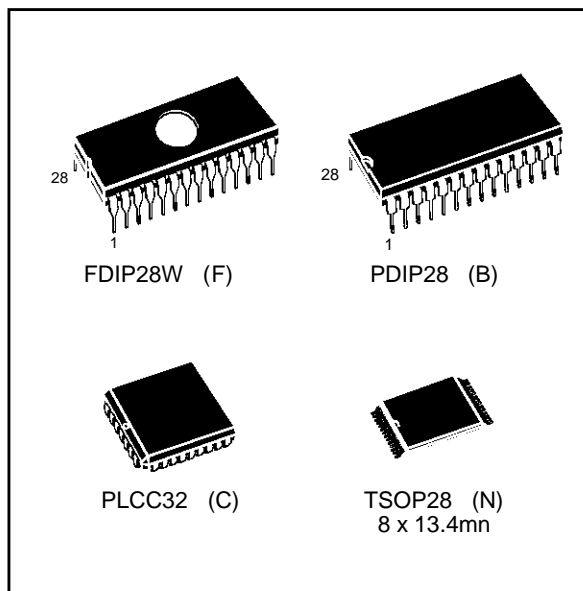
- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 3sec. (PRESTO II ALGORITHM)

### DESCRIPTION

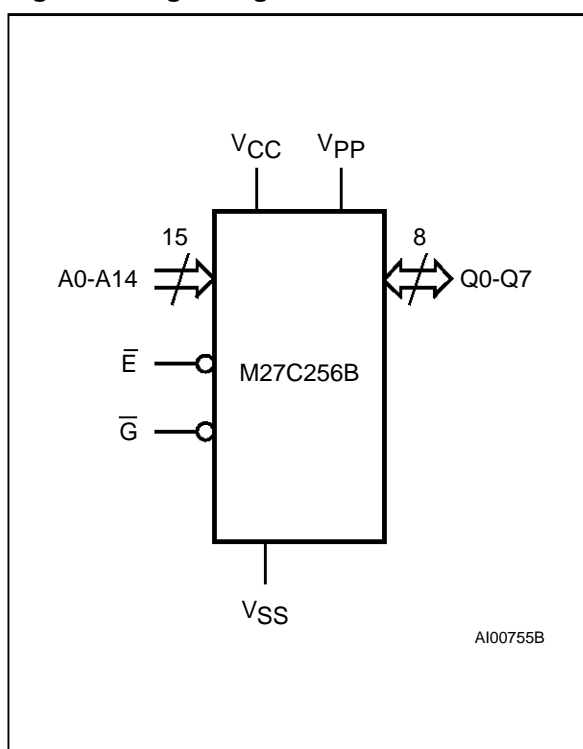
The M27C256B is a high speed 262,144 bit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems. It is organized as 32,768 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C256B is offered in Plastic Dual-in-Line, Plastic Leaded Chip Carrier, and Plastic Thin Small Outline packages.



**Figure 1. Logic Diagram**



**Table 1. Signal Names**

A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
$V_{PP}$	Program Supply
$V_{CC}$	Supply Voltage
$V_{SS}$	Ground

Table 2. Absolute Maximum Ratings <sup>(1)</sup>

Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Operating Temperature	−40 to 125	°C
T <sub>BIAS</sub>	Temperature Under Bias	−50 to 125	°C
T <sub>STG</sub>	Storage Temperature	−65 to 150	°C
V <sub>IO</sub> <sup>(2)</sup>	Input or Output Voltages (except A9)	−2 to 7	V
V <sub>CC</sub>	Supply Voltage	−2 to 7	V
V <sub>A9</sub> <sup>(2)</sup>	A9 Voltage	−2 to 13.5	V
V <sub>PP</sub>	Program Supply Voltage	−2 to 14	V

**Notes:** 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

2. Minimum DC voltage on Input or Output is −0.5V with possible undershoot to −2.0V for a period less than 20ns. Maximum DC voltage on Output is V<sub>CC</sub> +0.5V with possible overshoot to V<sub>CC</sub> +2V for a period less than 20ns.

Figure 2A. DIP Pin Connections

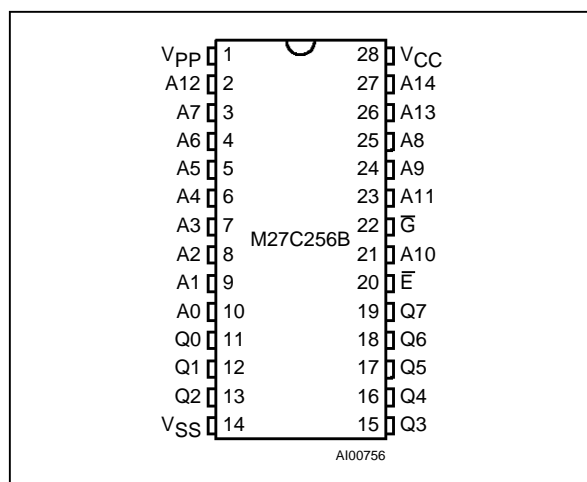
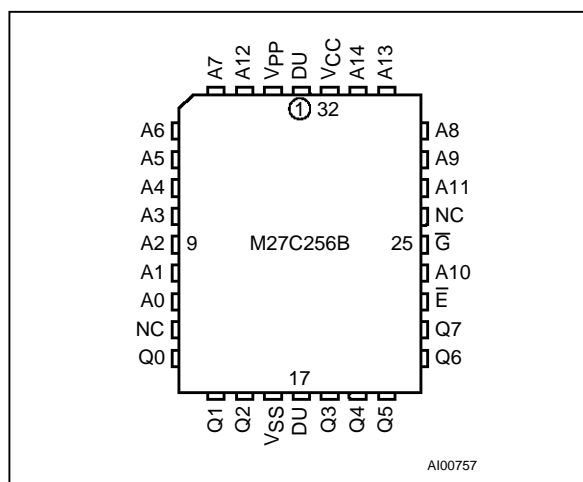
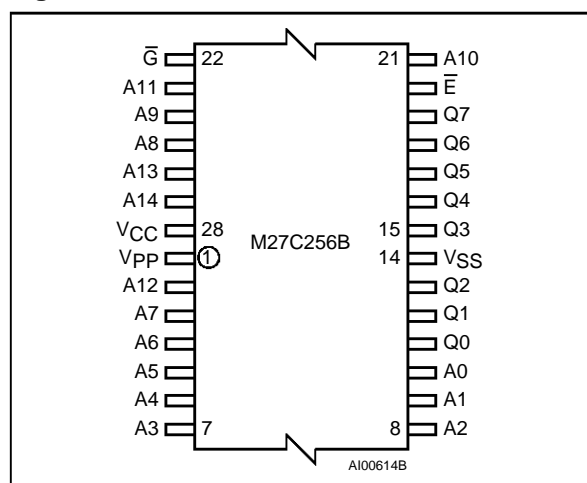


Figure 2B. LCC Pin Connections



**Warning:** NC = Not Connected, DU = Don't Use.

Figure 2C. TSOP Pin Connections



## DEVICE OPERATION

The modes of operation of the M27C256B are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V<sub>PP</sub> and 12V on A9 for Electronic Signature.

### Read Mode

The M27C256B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ( $\bar{E}$ ) is the power control and should be used for device selection. Output Enable ( $\bar{G}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time

**DEVICE OPERATION** (cont'd)

( $t_{AVQV}$ ) is equal to the delay from  $\overline{E}$  to output ( $t_{ELQV}$ ). Data is available at the output after delay of  $t_{GLQV}$  from the falling edge of  $\overline{G}$ , assuming that  $\overline{E}$  has been low and the addresses have been stable for at least  $t_{AVQV}-t_{GLQV}$ .

**Standby Mode**

The M27C256B has a standby mode which reduces the active current from 30 mA to 100  $\mu$ A. The M27C256B is placed in the standby mode by applying a CMOS high signal to the  $\overline{E}$  input. When in the standby mode, the outputs are in a high impedance state, independent of the  $\overline{G}$  input.

**Two Line Output Control**

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- the lowest possible memory power dissipation,
- complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines,  $\overline{E}$  should be decoded and used as the primary device selecting function, while  $\overline{G}$  should be made a common connection to all devices in the array and connected to the  $\overline{READ}$  line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

**System Considerations**

The power switching characteristics of Advance CMOS EPROMs require careful decoupling of the devices. The supply current,  $I_{CC}$ , has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of  $\overline{E}$ . The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1  $\mu$ F ceramic capacitor be used on every device between  $V_{CC}$  and  $V_{SS}$ . This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a

**Table 3. Operating Modes**

Mode	$\overline{E}$	$\overline{G}$	A9	$V_{PP}$	Q0 - Q7
Read	$V_{IL}$	$V_{IL}$	X	$V_{CC}$	Data Out
Output Disable	$V_{IL}$	$V_{IH}$	X	$V_{CC}$	Hi-Z
Program	$V_{IL}$ Pulse	$V_{IH}$	X	$V_{PP}$	Data In
Verify	$V_{IH}$	$V_{IL}$	X	$V_{PP}$	Data Out
Program Inhibit	$V_{IH}$	$V_{IH}$	X	$V_{PP}$	Hi-Z
Standby	$V_{IH}$	X	X	$V_{CC}$	Hi-Z
Electronic Signature	$V_{IL}$	$V_{IL}$	$V_{ID}$	$V_{CC}$	Codes

Note: X =  $V_{IH}$  or  $V_{IL}$ ,  $V_{ID}$  = 12V  $\pm$  0.5V

**Table 4. Electronic Signature**

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	$V_{IL}$	0	0	1	0	0	0	0	0	20h
Device Code	$V_{IH}$	1	0	0	0	1	1	0	1	8Dh

## AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	$\leq 20\text{ns}$
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

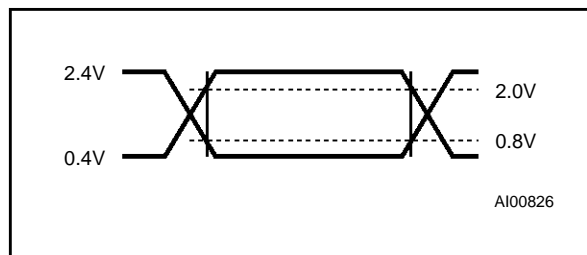
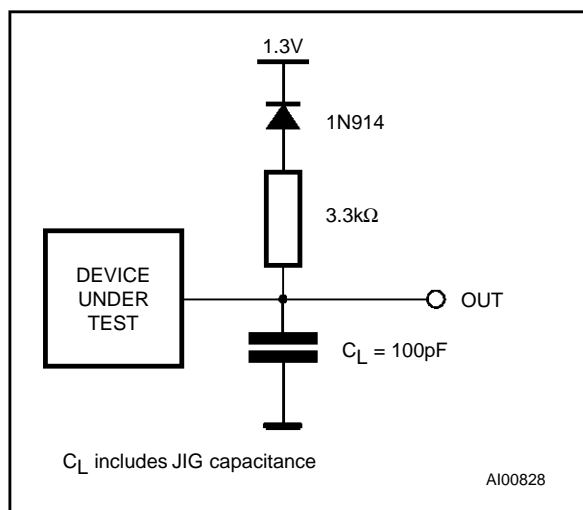


Figure 4. AC Testing Load Circuit

Table 5. Capacitance<sup>(1)</sup> ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Symbol	Parameter	Test Condition	Min	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0\text{V}$		6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0\text{V}$		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics<sup>(1)</sup>

( $T_A = 0$  to  $70^\circ\text{C}$ ,  $-40$  to  $85^\circ\text{C}$ ,  $-40$  to  $105^\circ\text{C}$  or  $-40$  to  $125^\circ\text{C}$ ;  $V_{CC} = 5\text{V} \pm 5\%$  or  $5\text{V} \pm 10\%$ ;  $V_{PP} = V_{CC}$ )

Symbol	Parameter	Test Condition	Min	Max	Unit
$I_{LI}$	Input Leakage Current	$0\text{V} \leq V_{IN} \leq V_{CC}$		$\pm 10$	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$0\text{V} \leq V_{OUT} \leq V_{CC}$		$\pm 10$	$\mu\text{A}$
$I_{CC}$	Supply Current	$\bar{E} = V_{IL}$ , $\bar{G} = V_{IL}$ , $I_{OUT} = 0\text{mA}$ , $f = 5\text{MHz}$		30	mA
$I_{CC1}$	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		1	mA
$I_{CC2}$	Supply Current (Standby) CMOS	$\bar{E} > V_{CC} - 0.2\text{V}$		100	$\mu\text{A}$
$I_{PP}$	Program Current	$V_{PP} = V_{CC}$		100	$\mu\text{A}$
$V_{IL}$	Input Low Voltage		-0.3	0.8	V
$V_{IH}^{(2)}$	Input High Voltage		2	$V_{CC} + 1$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1\text{mA}$		0.4	V
$V_{OH}$	Output High Voltage TTL	$I_{OH} = -1\text{mA}$	3.6		V
	Output High Voltage CMOS	$I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.7\text{V}$		V

Notes: 1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

2. Maximum DC voltage on Output is  $V_{CC} + 0.5\text{V}$ .

**Table 7A. Read Mode AC Characteristics <sup>(1)</sup>**(T<sub>A</sub> = 0 to 70°C, -40 to 85°C, -40 to 105°C or -40 to 125°C; V<sub>CC</sub> = 5V ± 5% or 5V ± 10%; V<sub>PP</sub> = V<sub>CC</sub>)

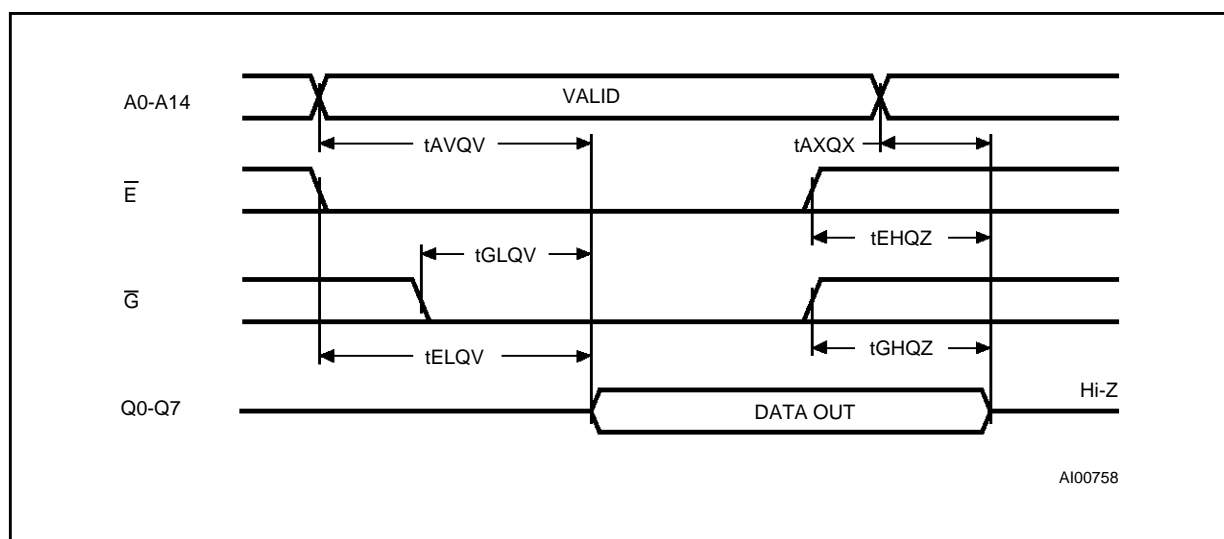
Symbol	Alt	Parameter	Test Condition	M27C256B						Unit
				-70		-80		-90		
				Min	Max	Min	Max	Min	Max	
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address Valid to Output Valid	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$		70		80		90	ns
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		70		80		90	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		35		40		40	ns
t <sub>EHQZ</sub> <sup>(2)</sup>	t <sub>DF</sub>	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	30	ns
t <sub>GHQZ</sub> <sup>(2)</sup>	t <sub>DF</sub>	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	30	ns
t <sub>AXQX</sub>	t <sub>OH</sub>	Address Transition to Output Transition	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$	0		0		0		ns

**Table 7B. Read Mode AC Characteristics <sup>(1)</sup>**(T<sub>A</sub> = 0 to 70°C, -40 to 85°C, -40 to 105°C or -40 to 125°C; V<sub>CC</sub> = 5V ± 5% or 5V ± 10%; V<sub>PP</sub> = V<sub>CC</sub>)

Symbol	Alt	Parameter	Test Condition	M27C256B						Unit
				-10		-12		-15/-20/-25		
				Min	Max	Min	Max	Min	Max	
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address Valid to Output Valid	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$		100		120		150	ns
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120		150	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		50		60		65	ns
t <sub>EHQZ</sub> <sup>(2)</sup>	t <sub>DF</sub>	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	40	0	50	ns
t <sub>GHQZ</sub> <sup>(2)</sup>	t <sub>DF</sub>	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	40	0	50	ns
t <sub>AXQX</sub>	t <sub>OH</sub>	Address Transition to Output Transition	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$	0		0		0		ns

**Notes:** 1. V<sub>CC</sub> must be applied simultaneously with or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.

2. Sampled only, not 100% tested.

**Figure 5. Read Mode AC Waveforms**

**Table 8. Programming Mode DC Characteristics <sup>(1)</sup>**(T<sub>A</sub> = 25 °C; V<sub>CC</sub> = 6.25V ± 0.25V; V<sub>PP</sub> = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I <sub>LI</sub>	Input Leakage Current	V <sub>IL</sub> ≤ V <sub>IN</sub> ≤ V <sub>IH</sub>		±10	μA
I <sub>CC</sub>	Supply Current			50	mA
I <sub>PP</sub>	Program Current	$\bar{E} = V_{IL}$		50	mA
V <sub>IL</sub>	Input Low Voltage		-0.3	0.8	V
V <sub>IH</sub>	Input High Voltage		2	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA		0.4	V
V <sub>OH</sub>	Output High Voltage TTL	I <sub>OH</sub> = -1mA	3.6		V
V <sub>ID</sub>	A9 Voltage		11.5	12.5	V

**Note:** 1. V<sub>CC</sub> must be applied simultaneously with or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.**Table 9. Programming Mode AC Characteristics <sup>(1)</sup>**(T<sub>A</sub> = 25 °C; V<sub>CC</sub> = 6.25V ± 0.25V; V<sub>PP</sub> = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t <sub>AVEL</sub>	t <sub>AS</sub>	Address Valid to Chip Enable Low		2		μs
t <sub>QVEL</sub>	t <sub>DS</sub>	Input Valid to Chip Enable Low		2		μs
t <sub>VPHL</sub>	t <sub>VPS</sub>	V <sub>PP</sub> High to Chip Enable Low		2		μs
t <sub>VCHL</sub>	t <sub>VCS</sub>	V <sub>CC</sub> High to Chip Enable Low		2		μs
t <sub>ELEH</sub>	t <sub>PW</sub>	Chip Enable Program Pulse Width		95	105	μs
t <sub>EHQX</sub>	t <sub>DH</sub>	Chip Enable High to Input Transition		2		μs
t <sub>QXGL</sub>	t <sub>OES</sub>	Input Transition to Output Enable Low		2		μs
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable Low to Output Valid			100	ns
t <sub>GHQZ</sub>	t <sub>DFP</sub>	Output Enable High to Output Hi-Z		0	130	ns
t <sub>GHAX</sub>	t <sub>AH</sub>	Output Enable High to Address Transition		0		ns

**Note:** 1. V<sub>CC</sub> must be applied simultaneously with or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.**DEVICE OPERATION** (cont'd)

4.7μF bulk electrolytic capacitor should be used between V<sub>CC</sub> and V<sub>SS</sub> for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

**Programming**

When delivered (and after each erasure for UV EPROM), all bits of the M27C256B are in the '1'

state. Data is introduced by selectively programming '0' into the desired bit locations. Although only '0' will be programmed, both '1' and '0' can be present in the data word. The only way to change a '0' to a '1' is by die exposition to ultraviolet light (UV EPROM). The M27C256B is in the programming mode when V<sub>PP</sub> input is at 12.75 V, and  $\bar{E}$  is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V<sub>CC</sub> is specified to be 6.25 V ± 0.25 V.

Figure 6. Programming and Verify Modes AC Waveforms

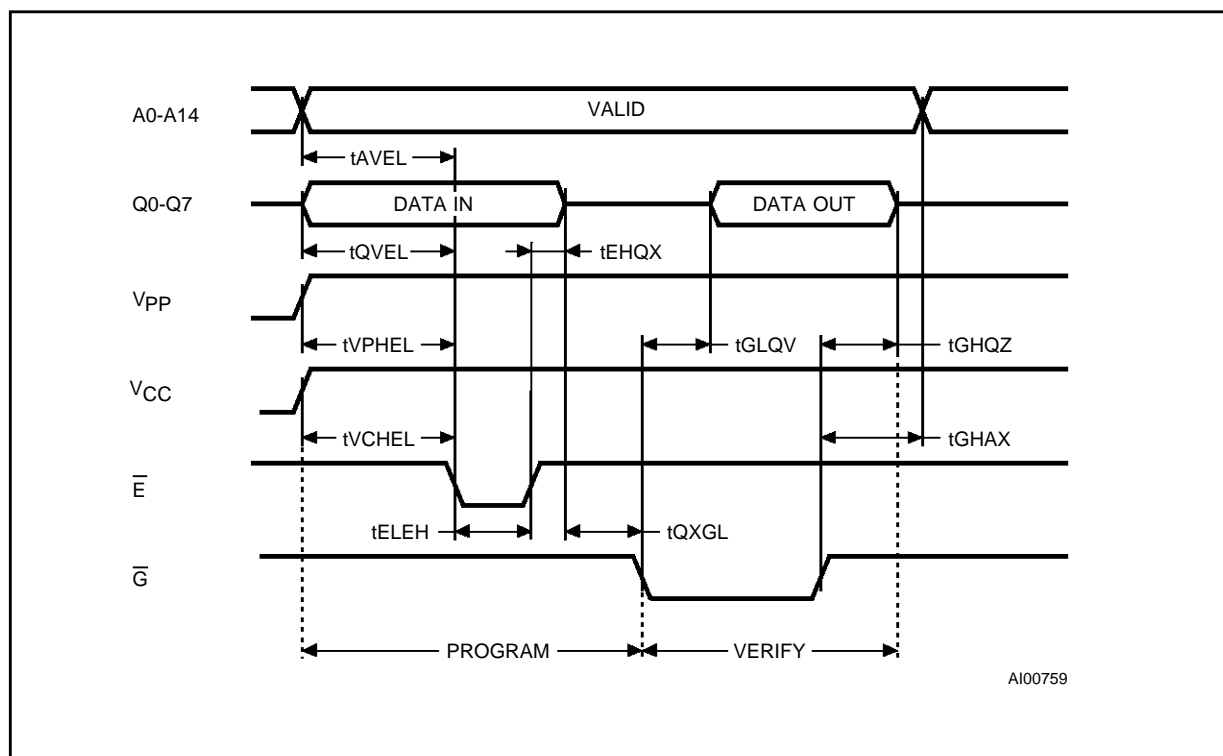
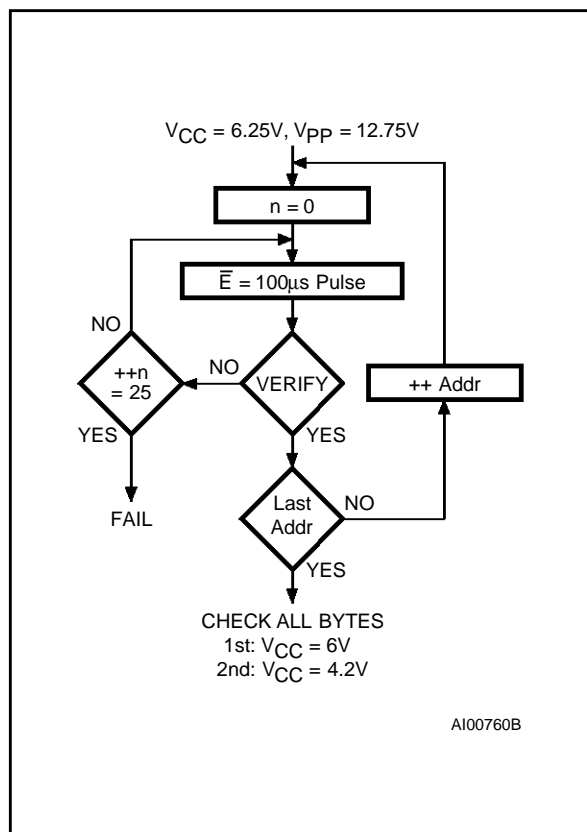


Figure 7. Programming Flowchart



### PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of 3.5 seconds. Programming with PRESTO II involves the application of a sequence of  $100\mu s$  program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

### Program Inhibit

Programming of multiple M27C256Bs in parallel with different data is also easily accomplished. Except for  $\bar{E}$ , all like inputs including  $\bar{G}$  of the parallel M27C256B may be common. A TTL low level pulse applied to a M27C256B's  $\bar{E}$  input, with  $V_{PP}$  at 12.75 V, will program that M27C256B. A high level  $\bar{E}$  input inhibits the other M27C256Bs from being programmed.

### Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with  $\bar{G}$  at  $V_{IL}$ ,  $\bar{E}$  at  $V_{IH}$ ,  $V_{PP}$  at 12.75V and  $V_{CC}$  at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C256B. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C256B, with V<sub>CC</sub> = V<sub>PP</sub> = 5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V<sub>IL</sub> to V<sub>IH</sub>. All other address lines must be held at V<sub>IL</sub> during Electronic Signature mode. Byte 0 (A0=V<sub>IL</sub>) represents the manufacturer code and byte 1 (A0=V<sub>IH</sub>) the device identifier code. For the SGS-THOMSON M27C256B, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C256B is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C256B in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C256B is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C256B window to prevent unintentional erasure. The recommended erasure procedure for the M27C256B is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm<sup>2</sup>. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm<sup>2</sup> power rating. The M27C256B should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C256B -70 X C 1 TR

Speed		V <sub>CC</sub> Tolerance		Package		Temperature Range		Option	
-70	70 ns	X	± 5%	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-80	80 ns	blank	± 10%	B	PDIP28	3	-40 to 125 °C		
-90	90 ns			C	PLCC32	6	-40 to 85 °C	TR	Tape & Reel Packing
-10	100 ns			N	TSOP28 8 x 13.4mm	7	-40 to 105 °C		
-12	120 ns								
-15	150 ns								
-20	200 ns								
-25	250 ns								

For a list of available options (Speed, V<sub>CC</sub> Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

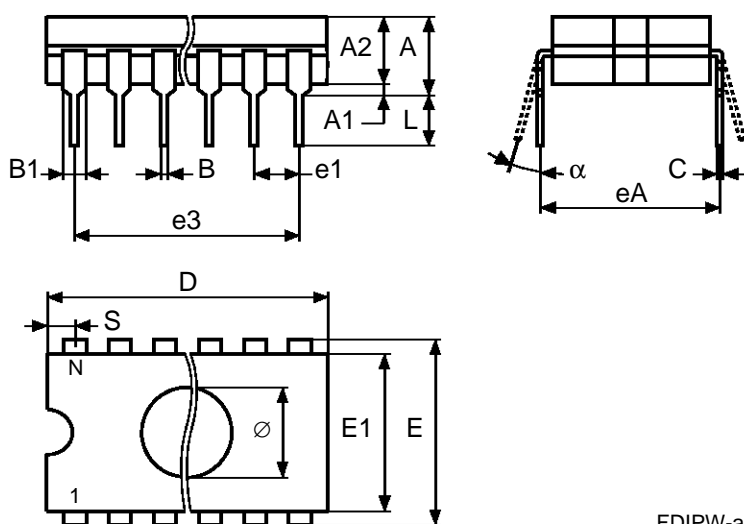
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.



**FDIP28W - 28 pin Ceramic Frit-seal DIP, with window**

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	—	—	0.100	—	—
e3	33.02	—	—	1.300	—	—
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
Ø	7.11	—	—	0.280	—	—
α		4°	15°		4°	15°
N		28			28	

FDIP28W

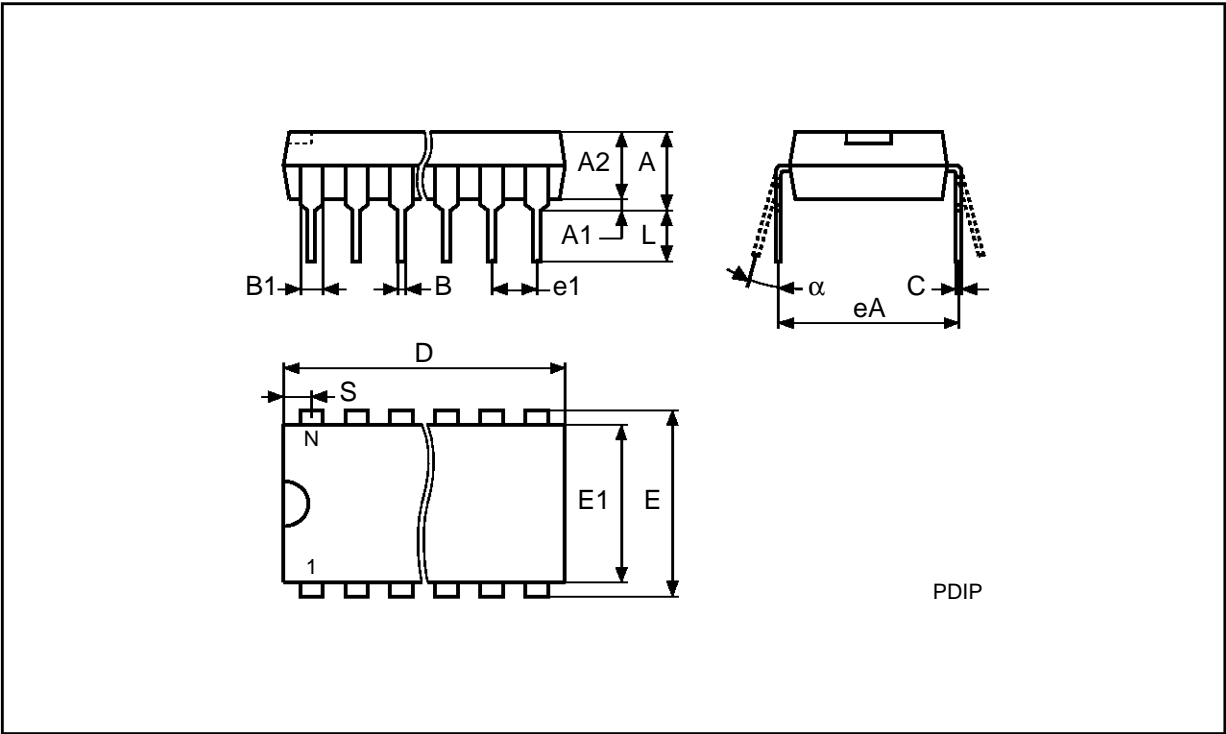


Drawing is not to scale

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	—	—	0.100	—	—
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28

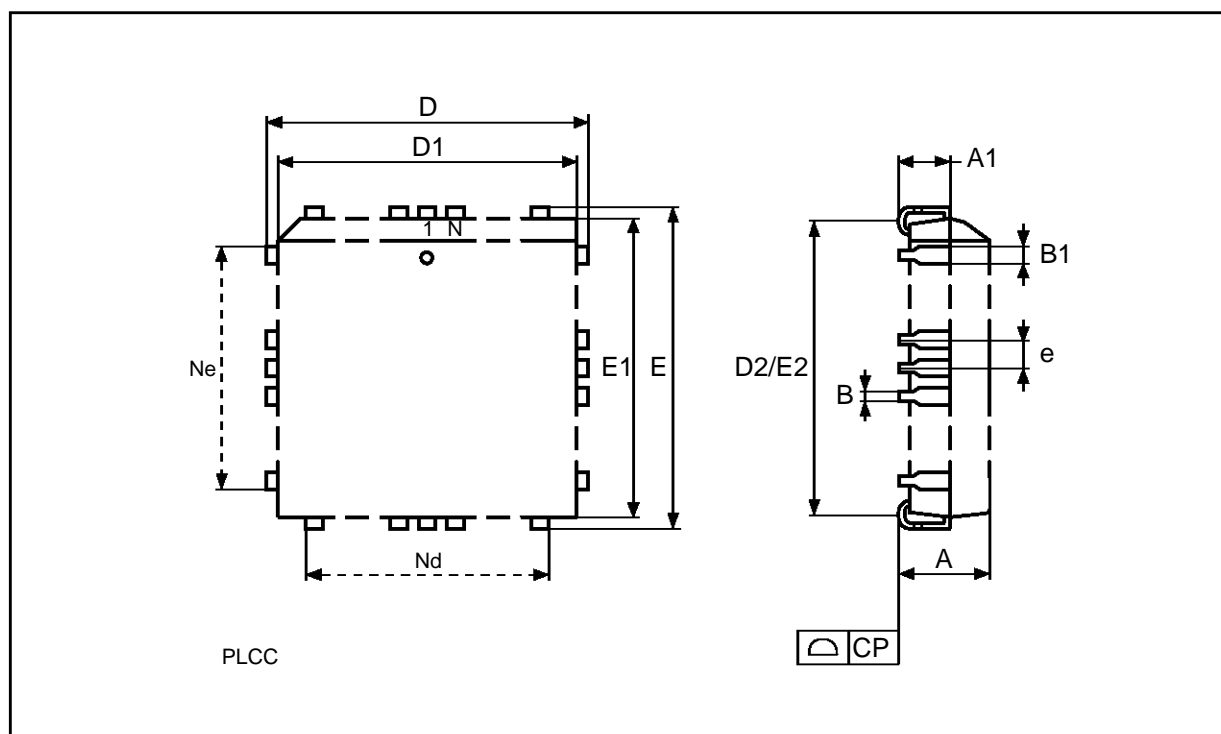


Drawing is not to scale

**PLCC32 - 32 lead Plastic Leaded Chip Carrier - rectangular**

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

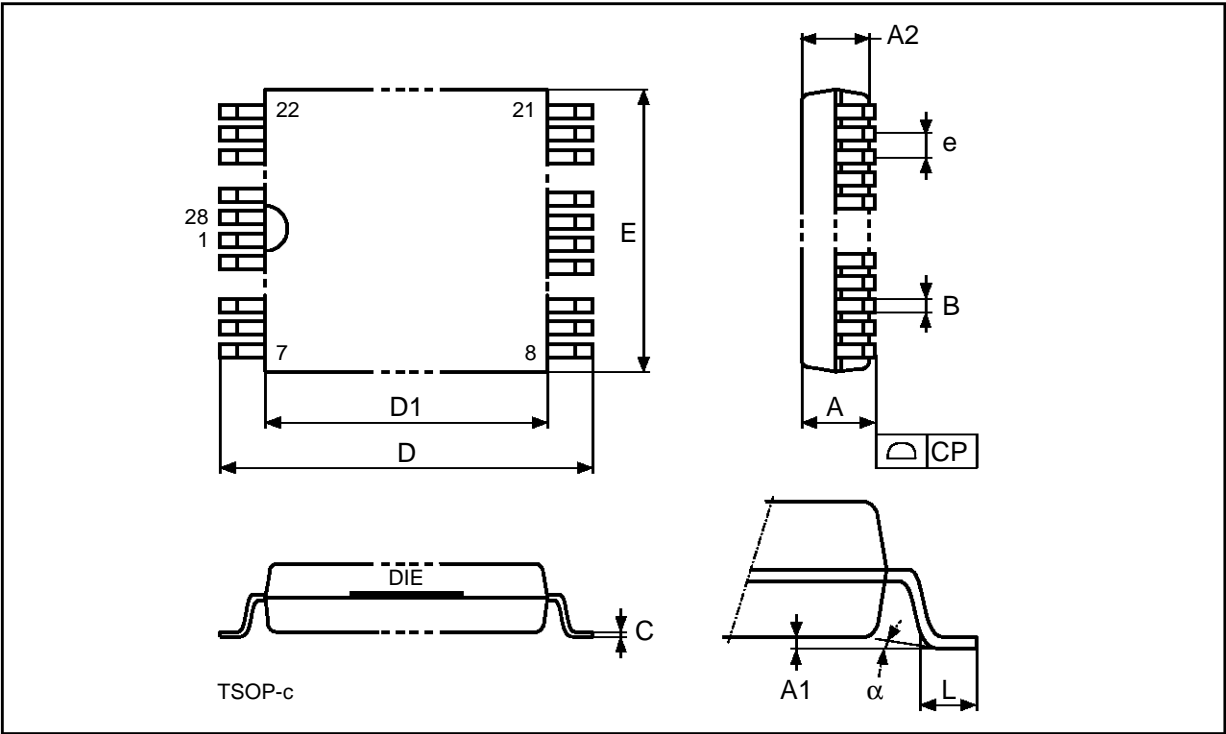


Drawing is not to scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.00	1.25		0.039	0.049
A1			0.20			0.008
A2		0.95	1.05		0.037	0.041
B			0.30			0.012
C		0.10	0.21		0.004	0.008
D		13.10	13.70		0.516	0.539
D1		11.70	11.90		0.461	0.469
E		7.90	8.25		0.311	0.325
e	0.55	-	-	0.022	-	-
L		0.30	0.70		0.012	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004

TSOP28



Drawing is not to scale

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